Double Feynman Gate (F2G) in Quantum-dot Cellular Automata (QCA)

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***Abstract*— Quantum dot Cellular Automata (QCA) is anticipated to allow for extremely dense nano-scale design and implementation of logic circuit over the Complementary Metal Oxide Semiconductor (CMOS). QCA has been considered as a promising alternative to CMOS technology for its lower power consumption, higher scale integration and higher switching frequency. Moreover, the basic element in QCA is majority gate. This paper present Double Feynman Gate (F2G) based on QCA logic gates: the QCA wire, MV gate and Inverter gate. The proposed circuit is designed and verified using QCADesigner.**

Keywords- *QCA, QCA Logic Gates, Double Feynman Gate (F2G), MV, Inverter gate*

I. INTRODUCTION

Now a day's, the use of Quantum technology is increased in various applications for its speed, size and power consumption [1, 2]. Quantum dot Cellular Automata is projected as a promising nanotechnology for future ICs [3, 4].

The basic element of QCA devices is the QCA cell shown in Figure 1(a). The basic structure in QCA is a cell that has four dots positioned at the corners of the squared cell and two mobile electrons. The basic idea of QCA is the physics of cell-to-cell interaction due to the rearrangement of electrons positions [5-10]. Depending on the position of the electrons, QCA cell has two type of polarization (p) [11-12]. A polarization of P=+1 (Binary 1) results if cells 1 and 3 occupied, while electrons on sites 2 and 4 result in P= -1 (Binary 0) as shown in Figure 1(b).

The cell polarization is defined [13] as Equation 1.

$$P = \frac{(\rho_2+\rho_4)-(\rho_1+\rho_3)}{(\rho_1+\rho_2+\rho_3+\rho_4)} \quad \text{..... (1)}$$

Where ρ_i denotes the electronic charge at dot i.

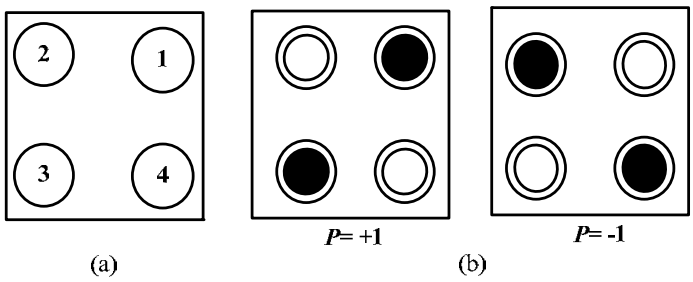


Figure 1: Basic Structure of QCA cell

II. QCA REVIEW

The fundamental unit of QCA-based design is wire, three input majority gate and inverter. QCA wire is an array of cells that are aligned one by one shown in Figure 2. The polarization of each cell in a QCA wire is directly affected by the polarization of its neighboring cells on account of electrostatic force. Accordingly, QCA wires can be used to propagate information from one end to another [14].

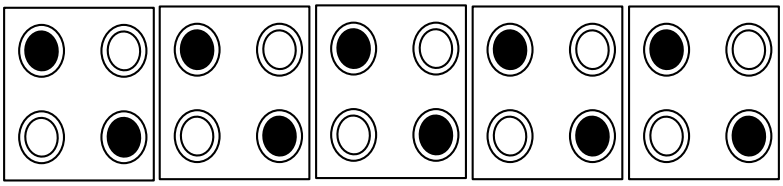


Figure 2**:** QCA wires

Three input Majority gate consists of five cells, three inputs, one output and a middle cell. The middle cell named device cell by reason of its function, switches to major polarization and determines the stable output. Majority gate can be programmed such that it functions as a 2-input AND or a 2-input OR by fixing one of the three input cells to p = -1 or p = +1, respectively shown in figure 3. The Boolean expression of majority gate is as follows:

MV (A, B, C) = AB+AC+BC

To make AND gate, we need to set one of the MV input is zero, Equation (2) presents the AND gate equation.

MV (A, B, 0) = AB+A.0+B.0= AB ……. (2)

To make OR gate, we need to set one of the MV input is 1, Equation (3) presents the OR gate equation.

MV (A, B, 1) = AB+A.1+B.1= A+B ……. (3)

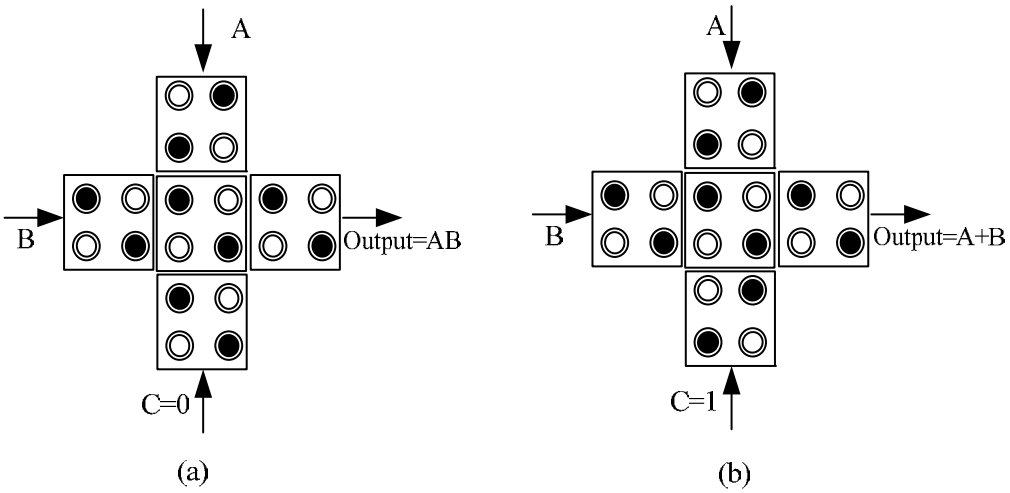


Figure 3: The QCA majority gate, function as (a) the AND gate and (b) the OR gate.

The inverting gate in QCA holds a different structure shown in Figure 4, since the last one (c) operates properly in all various circuits. This inverter is made of eight cell or four QCA wires. The input polarization is split into two polarizations and in the end, two wires join and make the reverse polarization.

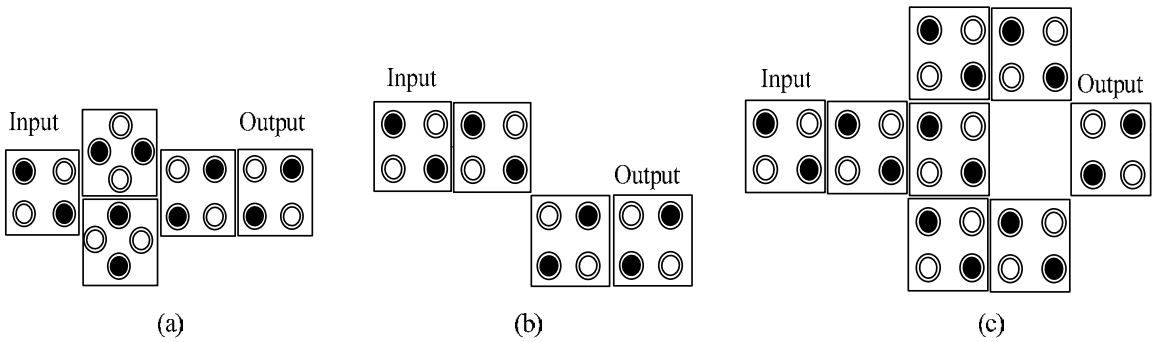


Figure 4: Three different structure of inverter gate

III. PROPOSED CIRCUIT AND PRESENTATION

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. In this paper we present one of the basic reversible logic gate "Double Feynman Gate (F2G)".

A. Double Feynman Gate

Figure 5 shows a 3*3 Double Feynman Gate [15]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P=A, Q=A⊕B, R=A⊕C. Table 1 represents the truth table of Double Feynman gate and figure 6 shows the block diagram of this gate in QCA.

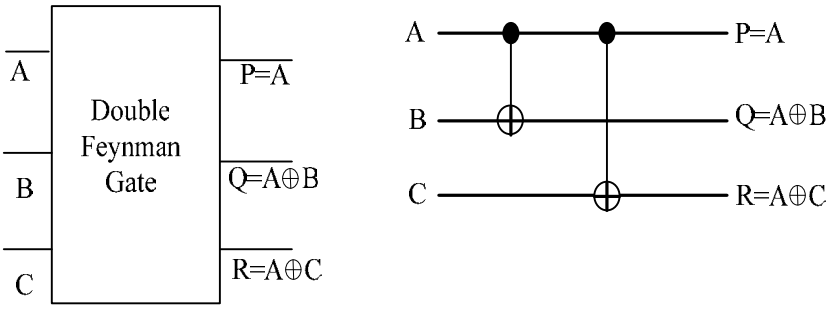


Figure 5: Double Feynman Gate

TABLE I. TRUTH TABLE OF DOUBLE FEYNMAN GATE

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

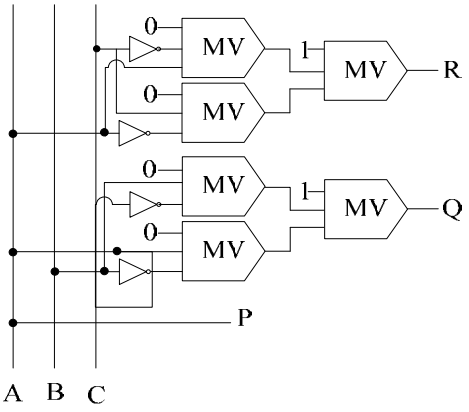
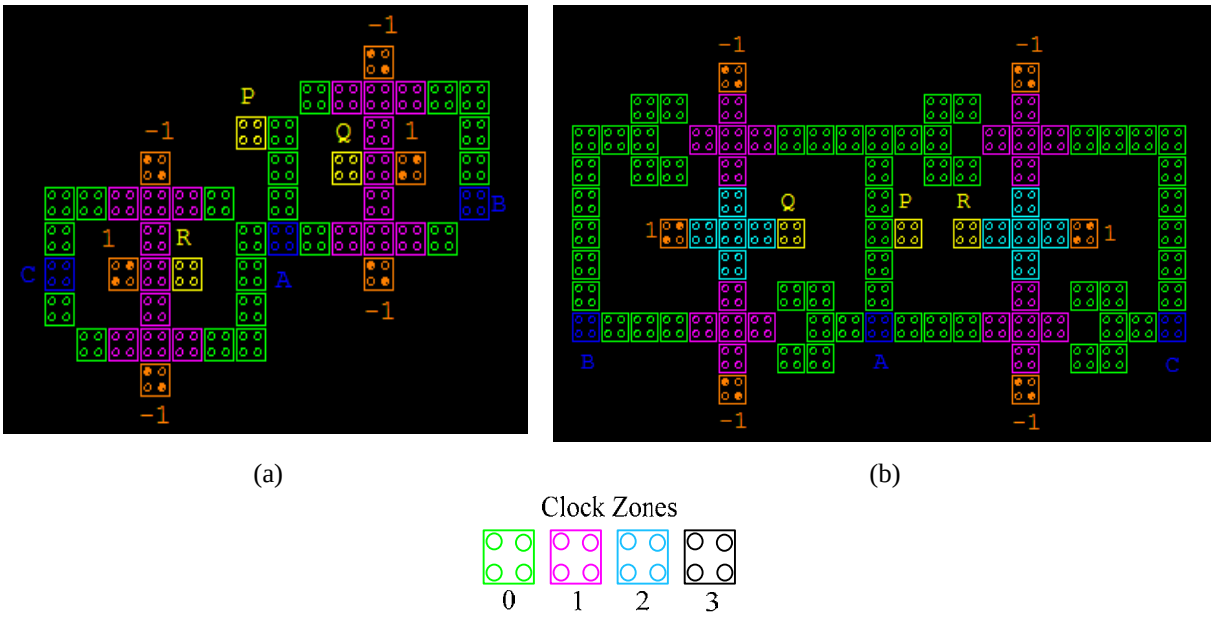


Figure 6: Block diagram of Double Feynman gate in QCA

IV. SIMULATION AND RESULT COMPARISION

Our proposed circuit was functionally simulated using the QCADesigner [16]. The following parameters are used for a Bistable Approximation: cell size=18nm, number of samples=50000, convergence tolerance=0.0000100, radius of effect=65.000000nm, relative permittivity=12.900000, clock high=9.800000e–022 J, clock low=3.800000e–023J, clock shift=0, clock amplitude factor=2.000000, layer separation=11.500000 and maximum iterations per sample=100. Most of the above mentioned parameters are default values in QCADesigner. Figure 7(a) and 7(b) shows two different structure of proposed circuit. In the Figure, the input signals are A, B, C and the output signal are P, Q and R. The figure 8 shows the input and output waveforms of our proposed circuit.

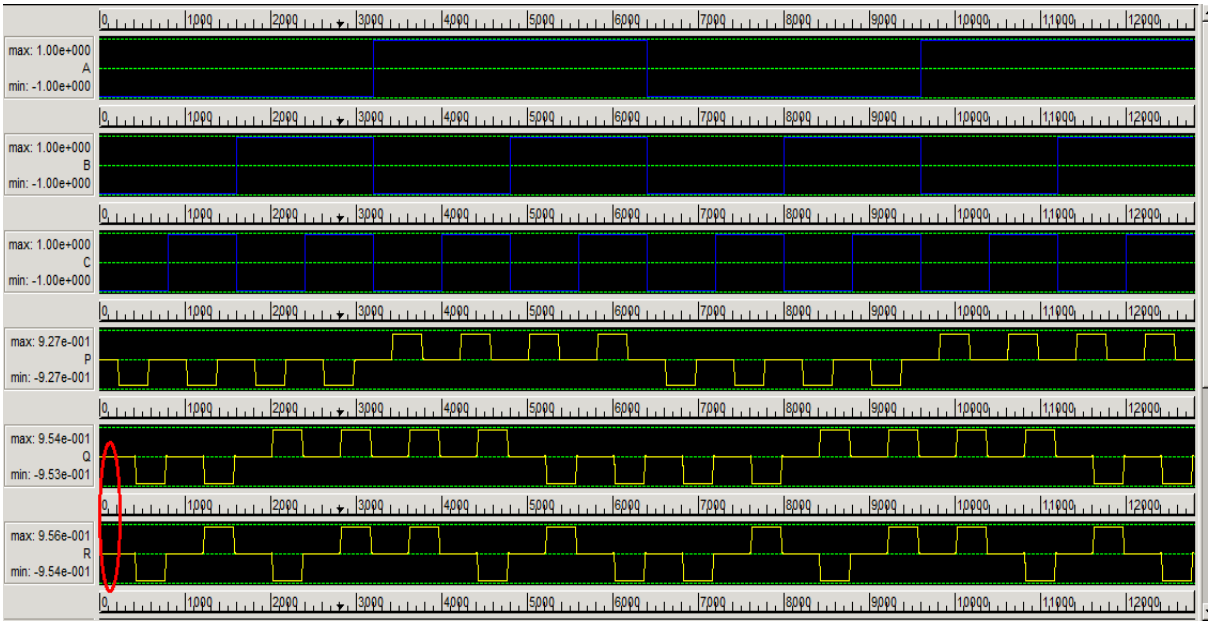


(a) (b)

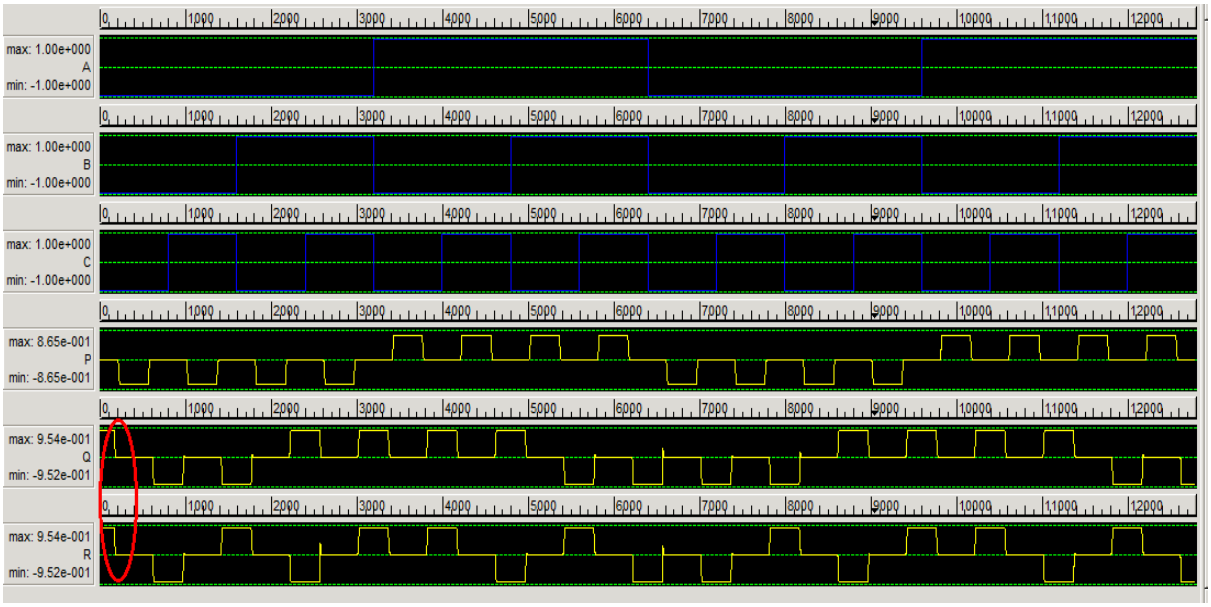
Figure 7: Double Feynman gate (a) designed by 51 cells, (b) designed by 96 cells

TABLE II. PERFORMANCE COMPARISON OF TWO PROPOSED LAYOUT

Parameter	Layout A	Layout B
Number of cells	51	96
Covered area (μm^2)	0.06	0.0924
Clock used	2	3
Time delay (clock)	0.5	0.75



(a)



(b)

Figure 8: Input output waveforms of Double Feynman gate (a) 0.50 clock cycle delay (b) 0.75 clock cycle delay

V. CONCLUSION

This paper presents a novel approach of designing Double Feynman gate (F2G) using quantum dot cellular automata technology. This proposed circuit has been simulated using QCADesigner and tested in terms of complexity (cell count) and area. The simulation result show that the proposed circuit performs well. The design is very useful for future computing techniques like ultra low power digital circuits and quantum computers.

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