A new low-power 1-Bit CMOS full-adder cell based on multiplexer

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Abstract: This paper presents a novel low-power and high-speed 1-bit full-adder, which is designed based on pass transistor and TG logics. The main advantage of this design is low propagation delay and lowpower consumption, which leads to achieving lower PDP than others. Intensive HSPICE simulation shows that the new full-adder consumes around 28.5% less power than 14T adder; moreover its PDPis 30% less than SS16T full-adder. We have compared two full-adders, 14T and SS16T, withour proposed full-adder. Simulation has been carried out by HSPICE in 0.18µm technology at 1.8V supply voltage.

Key words:TG,Pass-transistor,PDP, Propagation Delay.

1. Introduction

The highly increase of the demand of higher in processing speed and lower in power consumption electronic devices obliges designers to discover the innovative ways to meet these goals. Likewise, the more we scrutinize this complex and modernized century, the more we provide the spaces for challenging the problems which have been made because of unfair proportion of rapid growth of market's demand and the time-consuming nature of accomplishing new technologies.

The immense applications of VLSI such as e.g. microprocessors, Digital Signal Processors (DSP), etc. enormously exploit more arithmetic operations compared to logical operations. The focal core of all arithmetic blocks is considered as 1-bit Full-Adder cell. Therefore, it can be noted that the improvement of overall performance of the mentioned is resulted from developing this base block. In fact, the main concern for designers on the highly close relationship with the complexities of power consumption as well as architecture factors is associated with transistor count i.e. the number of used transistors per base block.

As regard to submicron CMOS technology area, it can be concluded that the topology selection, power dissipation and speed are taken into consideration as the most important characteristics of high speed and low power applications [1]. The result of lower supply voltage For CMOS circuits would be at the lower performance level. Furthermore, this performance loss can somehow be limited by scaling the threshold voltage resulting in increased leakage [6], [7]. Clock gating and dynamic voltage/frequency scaling are two other techniques applying in low power design [7-9]. Here, sub-threshold circuit design is to scale the supply voltage below the threshold voltage, in which the charged/discharged sub-threshold leakage currents are made through load capacitances. In this study, there exists an important restrain on the increased performance of sub-threshold circuits since leakage currents are considered as orders of magnitude lower than drain currents in the strong inversion regime. Hence, conventionally, we enjoyed the sub-threshold circuits for applications which necessitate ultra-low power dissipation, with low to moderate circuit performance [7], [9]. Likewise, one of the key constituents of a processor which establishes its throughput is the 1-bit full adder design since it is applied in ALU, the floating point unit, and direct generation towards the case of cache or memory accesses[7],[9].

The total power dissipated in generic digital CMOS gate is calculated by Eq. (1), Eq. (2), Eq. (3), and Eq. (4).

$$P_{Total}=P_{Dynamic}+P_{ShortCircuit}+P_{Static} \quad (1)$$

$$P_{Dynamic}=P.C_L.f.V_{DD}^2 \quad (2)$$

$$P_{ShortCircuit}=I_{peak}.t_{SC}.V_{DD}.f \quad (3)$$

$$P_{Static}=I_{Static}.V_{DD} \quad (4)$$

The mentioned variables in the above equations are respectively as follow: P as change state probability of gate, f as simulation frequency, C_L as capacitor of gate, V_{DD} as supply voltage, I_{peak} as maximum current during changing the status of gate, t_{SC} as short circuit time and I_{Static} as static current.

Static power is highly significant in low supply voltage. V_{th} modification and also the supply voltage reduction influence the circuit latency immediately, though the mitigating of supply voltage as well the modification of the threshold voltage give rise to reduction in the power consumption as shown in Equation (5), and Equation (6), any increase in V_{th} or reduction in supply voltage is likely to reduce circuit performance [12], [13].

$$T_{Propagation}NMOS = T_{P_{H\to L}} \approx \frac{C_L.V_{DD}}{K_n(V_{DD}-V_{tn})^2} \quad (5)$$

$$T_{Propagation}PMOS = T_{P_{L\to H}} \approx \frac{C_L.V_{DD}}{K_p(V_{DD} - |V_{tp}|)^2} \quad (6)$$

It can be figured out from published literatures that there exist lots of full-adders designed by using variety of logic techniques see. Of these adders, this paper addresses the following explained circuits for the purpose of comparison. Excluding the fact that all of these adders have the same functionality, they literally enjoy various intermediate nodes and outputs production method, the loads on them and also transistor count.

Indeed, all these full-adders tried to decrease the amount of power and delay factor. Thus, they reduce power delay product (PDP) compared to each presented full-adder.

Hence, the rest of the paper is organized as follows: Brief explains of two full-adders cells SS16T and 14T is presented in Section (2). Illustrate of proposed full-adder (MUAfull-adder) in Section (3). Thesimulation results of the proposed full-adder (MUAfull-adder) and performance comparisons with counterparts' full-addersare shown in Section (4). Finally, conclusion is given in Section (6).

2. Explain about two standard Full-Adders

2.1. SS16T Full-adder cell:

SS16T full-adder is as shown in Fig.1 [14]. It is based on pass-transistor, for design this adder uses 16 transistors. This adder it has lower propagation delay and decrease number of transistor than two previous adders, but it consume more power consumption.

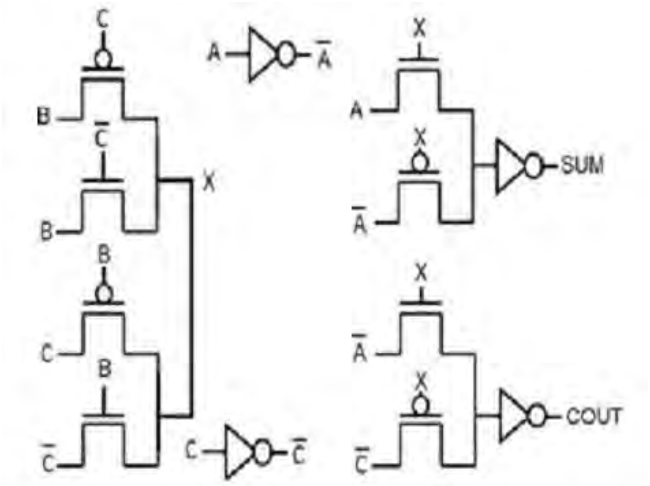

Fig. 1:SS16T full-adder [14]

2.2. 14T Full-Adder Cell

14T full-adder is as shown in Fig. 2 [15]. It is incorporation of pass-transistor and TG techniques and it has 14 transistors in its structure. This full-adder has the least number of transistors among all full-adders in this paper moreover it has very low propagation delay, but its problem is high power consumption.

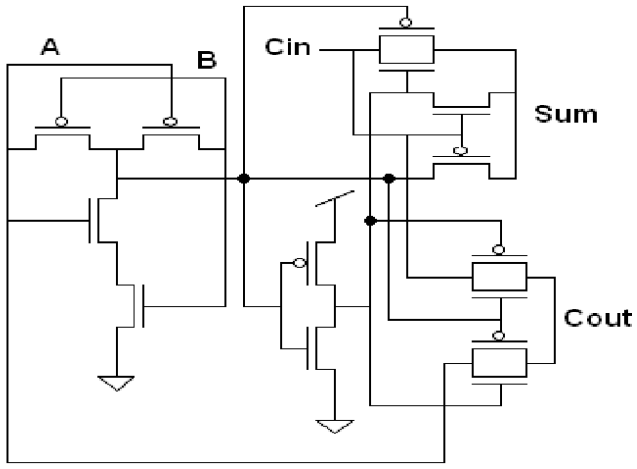

Fig. 2:14T full-adder [15]

3. Proposed Full-Adder Cell (MUAFull-AdderCell)

The proposedfull-adder is used20 transistors with minimum area. This full-adderis designed based on two logics of pass transistor and transmission gate (TG). This adder illustrate in Fig. 3. In this design our effort was on reducing power and delay, and the most advantage of this adder is low-power consumption. This proposed adder has low propagation delay and thus we intensive achieved the least power delay product (PDP).

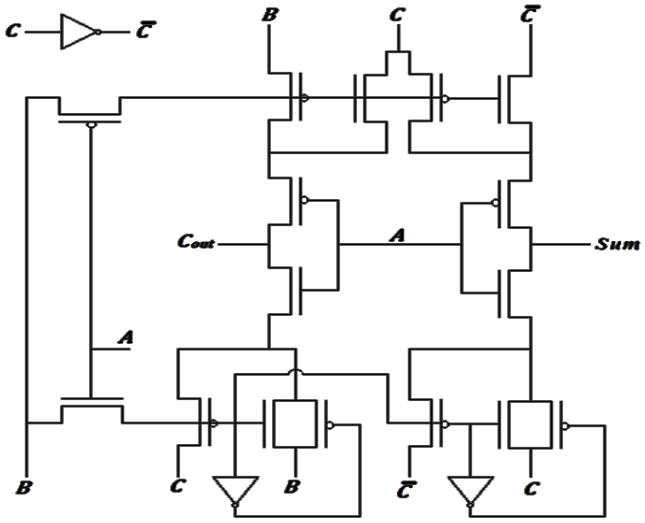

Fig. 3: The circuit of proposed Full-Adder Cell (MUAFull-Adder Cell)

4. Simulations and Results

In this section, the evaluation and comparison of the proposed circuit with other ones are done. The simulations have been done under same conditions for both mentioned full-adders as well as our design as follow: Utilizing 0.18µm CMOS technology files with 100MHz at 27^0C and applying 1.8 V as power supply.Table 1 represents the simulation results.

Table 1: Simulation results of full-adders based on 0.18 µm technology and the supply voltage of 1.8 V.

Design	Average power(µW)	Delay(PS)	PDP (FJ)
SS16T	49.69	119.85	5.955
14T	63.308	68	4.304944
Proposed Adder(MUA)	45.321	91.85	4.1627

As seen in Table 1 and Table 2, the MUA Full-Adder has the lowest power consumption and power delay product (PDP). In this design, we could reduce power consumption and PDP. Based on the results of the simulations, the proposed Full-Adder can be considered as the best Full-Adder in this paper.

5. Conclusions

In this paper, a novel low-power and low propagation delayfull-adderhas been proposed. The proposed circuit uses 20 transistors. Good design lead to reduction in power consumption and propagation delay. This full-adder has the lowest power consumption, and PDP than others. Simulation have been performed on HSPICE by using a 0.18µm technology two evaluate the new design (MUA adder) and two other adders, including 14T and SS16T full-adder. Simulation results show the presented adder has the best power consumptionand PDP in comparison with the others. This adder consumes around 28.5% and 9% less power compared with 14T and SS16T respectively.

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