Design and Analysis of 8T/10T SRAM cell using Charge Recycling Logic

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Abstract

Normally charge recycling (CR) logic is used to reduce power in SRAM memory cells.The read access time of 8T SRAM cell is slightly degraded in read "0'' operation. When the cell is in zero state, the bitline discharge along BT takes longer due to lower conductance of NMOS transistor.Two 4X4 SRAM macros have been implemented in a standard 180 nm CMOS process using the 8T and the 10T cells. Both macros have identical address decoders, data-line drivers and sense amplifier design. Extensive Read/Write operations have been simulated at 25,50,75 and 100° C to evaluate the performance of the proposed design. All the circuits simulations are designed with 250 MHz and 300 MHz operating frequency with supply voltage of 3.3 mV. It is apparent that at both operating frequencies, the proposed 10T SRAM design has significantly less read power consumption. This is because only one cell is turned on instead of all the cells in one row in the conventional design. The static and dynamic power also calculated for the two SRAM design with various temperature ranges.

Keywords-SRAM cell ;8T/10T memory cell;CR logic;CMOS Technology

I. INTRODUCTION

Once the write operation in a memory cell is completed next information to be ready to read the data. Assume that the content of the memory is a 1, stored at Q. The read cycle is started by pre-charging both the bit lines to a logical 1, then asserting the word line WL, enabling both the access transistors. The second step occurs when the values stored in Q and Q" are transferred to the bit lines by leaving BL at its pre-charged value and discharging BL" through M1 and M5 to a logical 0 (i.e. eventually discharging through the transistor M1 as it is turned on because the Q is logically set to 1). On the BL side, the transistors M4 and M6 pull the bit line toward VDD, a logical 1 (i.e. eventually being charged by the transistor M4 as it is turned on because Q is logically set to 0) in Figure4.1. If the content of the memory was a 0, the opposite would happen and BL would be pulled toward 1 and BL toward 0. Then these BL and BL will have a small difference of delta between them and then these lines reach a sense amplifier, which will sense which line has higher voltage and thus will tell whether there was 1 stored or 0. The higher the sensitivity of sense amplifier, the faster the speed of read operation.

II. READ OPERATION

When a read operation is issued the memory cell will go through the following steps.

1)Bit-line Pre-charging: For a read, BL pre-charged to VDD, and then floated. Since, in idle mode BL maintained at VDD, this step didn''t include any dynamic energy consumption.

2)Word-line activation: in this step word-line 2 asserted to GND and two states can be considered:

(a) Voltage of ST node is low: when, voltage of ST node is low, the voltage of BL pulled down to low voltage by PMOS access transistor. We refer to this voltage of BL as VBL-Low.

(b) Voltage of ST node is high: when voltage of ST node is height, the voltage of BL and ST node equalized (we refer to voltage of BL in this state as VBL-High). Since in this state, there is very small different between BL and ST node, dynamic energy consumption is very small.

3) Sensing: After word-line2 deactivate the sense amplifier is turned on to read data on BL. Fig. 3 shows circuit schematic of sense amplifier that used for reading data from new cell.

4) Idle mode: At the end of read operation, cell will go to idle mode and word-line2 and BL asserted to VIdle2 and VDD, respectively.

Considering the case of reading Q=0; before reading a value from the storage nodes, the bit line BL is pre-charged to VDD. The read word line RL is then asserted to VDD. The storage node Q'' that stores a 1 is

statically connected to the gate of MRA (Read Access Transistor) and will drain the charges on the bit line through MRD to GND as the RL is 1, which means that the bit line has just read a 0. On the contrary, when Q=1, Q'‘ will be 0 and MRA will be in cutoff and the bit line BL would not be able to discharge through MRD to Gnd, and it would read a 1. [3]

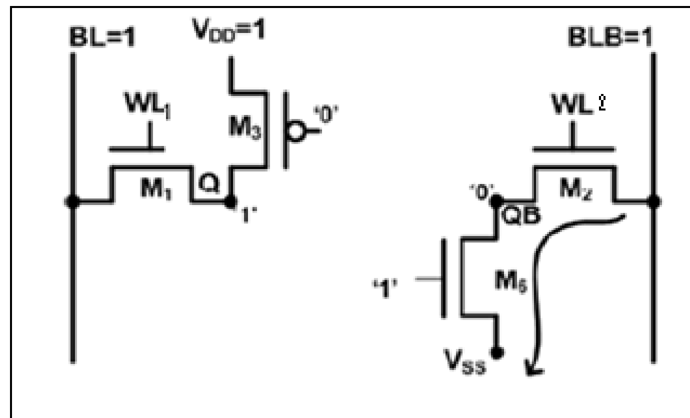

Figure 1. Read Operation of a conventional 6T SRAM cell

III. Read Operation of 8T SRAM cell

The read access time of 8T SRAM cell is slightly degraded in read "0'‘ operation. When the cell is in zero state, the bitline discharge along BT takes longer due to lower conductance of NMOS transistor.

IV. Banked Organization Of SRAM Cell For Read Operation

Banking is an organization technique that targets total switched capacitance to achieve reduced power and improved speed. Our previous design of the SRAM memory core shows that an n-bit memory needs a R X C memory core, where R is the number of rows and C is the number of columns. An unfortunate outcome of such an organization is that any access to the core causes R cells to be enabled and the entire set of bit lines to be toggled. In general, if C_{cell} is the capacitance of the bit line per cell, a total capacitance of R X C X C_{cell} is switched. In this design 4X4 SRAM memory is designed to write a 2 bit information in memory shown in Figure 4.3.

Each block of the array is of 10T SRAM cell. There are 4 rows and 4 columns arranged to form a 4x4 SRAM cell array. To address these rows of cells, the decoder is used prior to the array arrangement. As the row consists of 4 cells it constitutes to form half a byte. The AND based 2:4 decoder is used to generate the address lines, the number of transistors used for the decoder circuit is 28 These address lines which form the outputs of decoder are connected to each row of the array.

The input and output data control consists of write and ready circuitry. From the decoder the address is selected in the array and 4 bits of data is written or read in parallel from cell 1 to cell 4 shown in Figure 6. Input-output buffers are also required for each column as the decoder selects only one row of the array, the other cells may generate glitch, this can be nullified by the buffers. Also a 8x1 Multiplexer can be used to combine all the output of single SRAM cells of each column to make a single output data. The Figure 2 shows the 4x4 SRAM cell array design consists of 10T one bit SRAM cell, decoders and buffers. The total number of transistors utilized in this 4x4 SRAM cell array is 172[10].

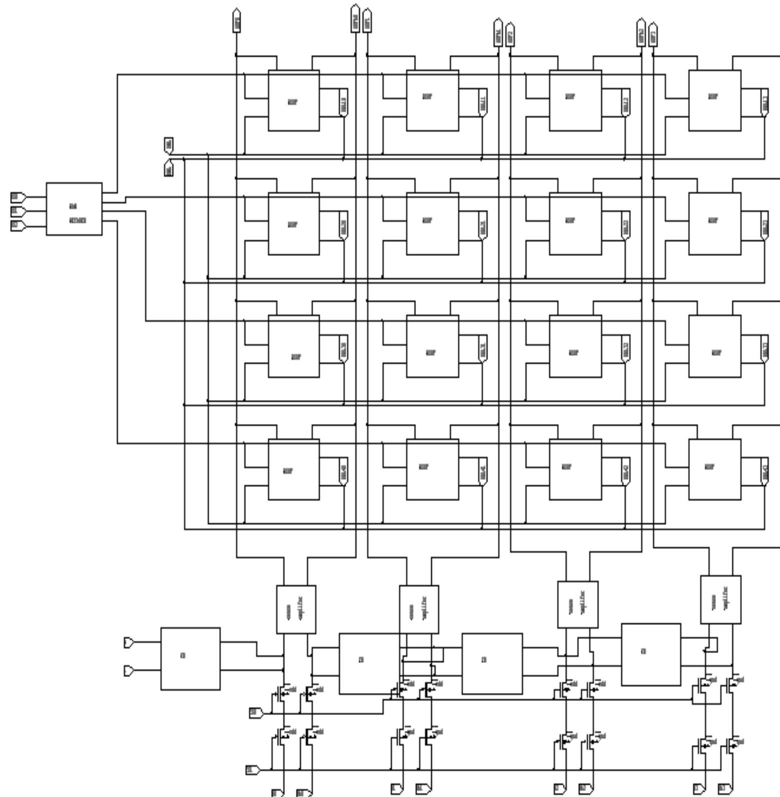

Figure 2. SRAM Read operation of 4X4 of 8T SRAM

V. DESIGN OF 4X4 SRAM MEMORY CELL

At initial stage of read operation, decoder will be in inactive mode. As soon as decoder is enabled, they are pre-charged first. This process makes all output high for a small amount of time. This address is invalid then address settles down according to the input of the decoder and one particular SRAM cell is activated. Activation of read enable (RE) signal activates the read buffer[3].The ready SRAM cell data traverses towards ready buffer.Thus the data bit is read from memory cell. To continue the read operation address bits are changed to address the next memory cell. During write operation, the address is selected and data is given to write circuit as input. Upon the activation of write enable (WE) signal activates the write buffer output change according to the input. The feedback action in SRAM cell then stabilizes the data of the memory.This signal is disabled for safe write operation and to avoid further writing of spurious data. To continue the write operation to other cells address bits are changed and same procedure is repeated again and again for required times.

VI. DESIGN OF 10T SRAM MEMORY CELL

At initial stage of read operation, decoder will be in inactive mode. As soon as decoder is enabled, they are pre-charged first. This process makes all output high for a small amount of time. This address is invalid then address settles down according to the input of the decoder and one particular SRAM cell is activated. Activation of read enable (RE) signal activates the read buffer[3].

The ready SRAM cell data traverses towards ready buffer.Thus the data bit is read from memory cell. To continue the read operation address bits are changed to address the next memory cell. During write operation, the address is selected and data is given to write circuit as input. Upon the activation of write enable (WE) signal activates the write buffer output change according to the input. The feedback action in SRAM cell then stabilizes the data of the memory.This signal is disabled for safe write operation and to avoid further writing of spurious data. To continue the write operation to other cells address bits are changed and same procedure is repeated again and again for required times.The Figure 4.6 and 4.7 shows the simulated output of 4x4 SRAM cell array for both write and read operations[5,6].

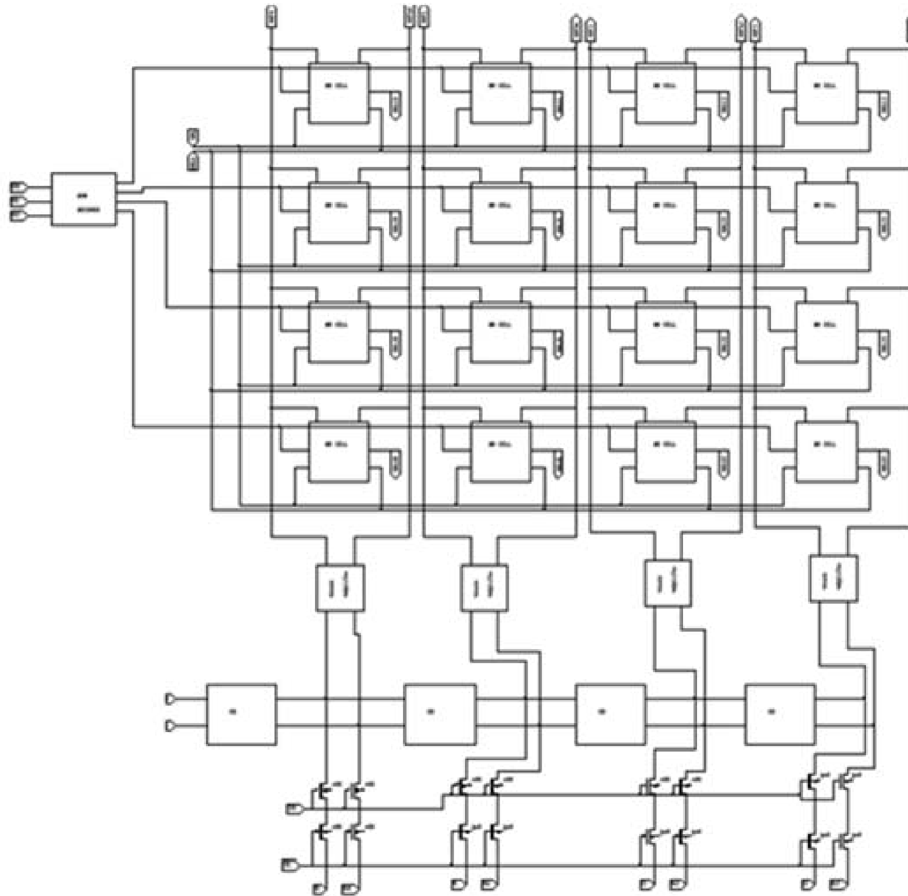

Figure 3. Design of 4X4 SRAM memory cell for 10T SRAM cell

VII. READ PERFORMANCE IN SRAM CELL

Two 4X4 SRAM macros have been implemented in a standard 180 nm CMOS process using the 8T and the 10T cells. Both macros have identical address decoders, data-line drivers and sense amplifier design. Extensive Read/Write operations have been simulated at 100° C to evaluate the performance of the newly proposed cell. All results are calculated at 250 MHz and 300 MHz operating frequency and 3.3 mV supply. It is apparent that at both operating frequencies, the proposed design has a significantly less read power consumption. This is because only one cell is turned on instead of all the cells in one row in the conventional design. The static and dynamic power also calculated for the two SRAM design with various temperature ranges.

VIII. SIMULATION RESULTS

Figure 4 shows the CR logic to improve the read operation of 8T SRAM cell.A slight modification in conventional 8T SRAM circuit to improve its speed of response.

The CR logic allows NOR gates instead of normal transitors to improve the performance.Only area overhead take place in case of increase in transistors.The modified circuit shown in Figure 6 for 10T SRAM cell for read operation.

The Figure 5 shows the simulated output of 4x4 SRAM cell array for both write and read operations using banked organization architecture.The same design can be implemented for any SRAM array structure.

Figure 7 depicts the output waveform across 4x4 SRAM memory cell.The read operation performance increases as compared to normal read circuit in 10T SRAM memory cell.

Table 1 and shows various power calculation at different temperature conditions for input voltage range 0 to 1.8V in 8T SRAM cell Table 2 shows various power calculations at different temperature conditions for input voltage range 0 to 1.8V for 10T SRAM cell.

From the above tables we found that when temperature increases from 0°C the total power increases with respect to time. Dynamic and static power remains constant for greater temperature range.[14,15] Transient time increases so total time of the write and read circuit increases, thereby speed of operation also increases.

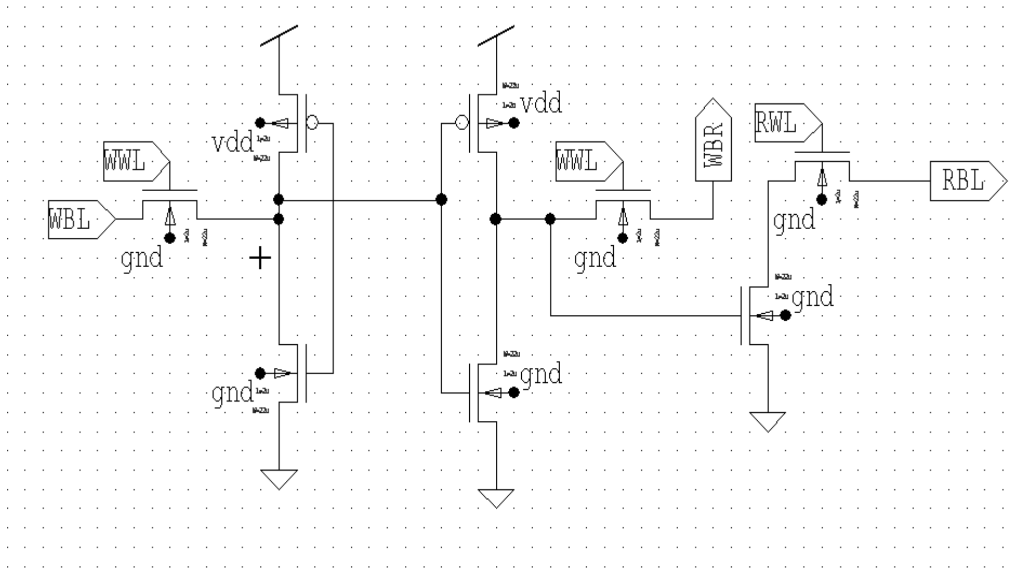

Figure 4. CR logic for 8T SRAM memory cell

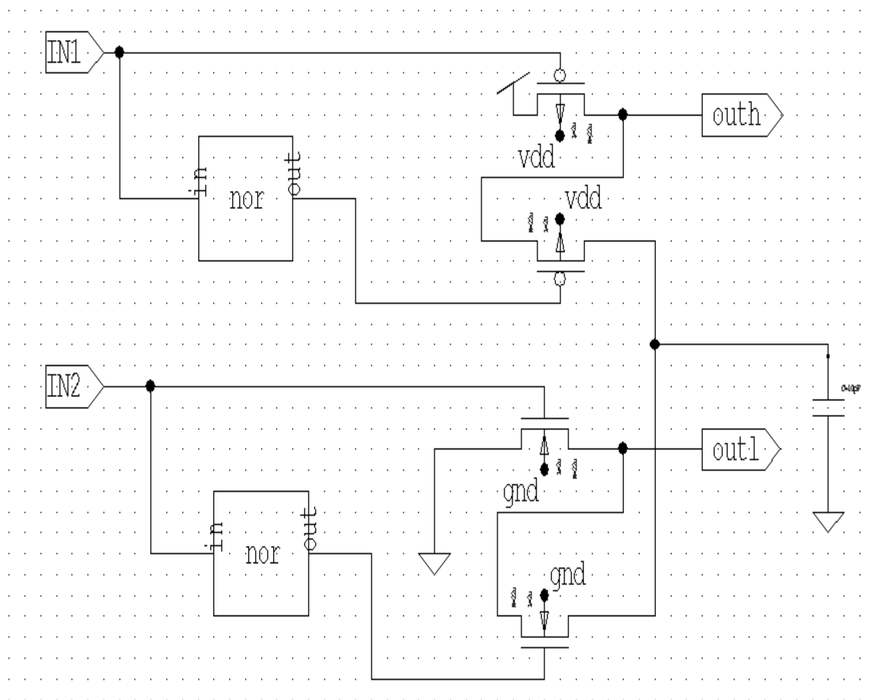

Figure 5. Design of 10T SRAM cell for read operation

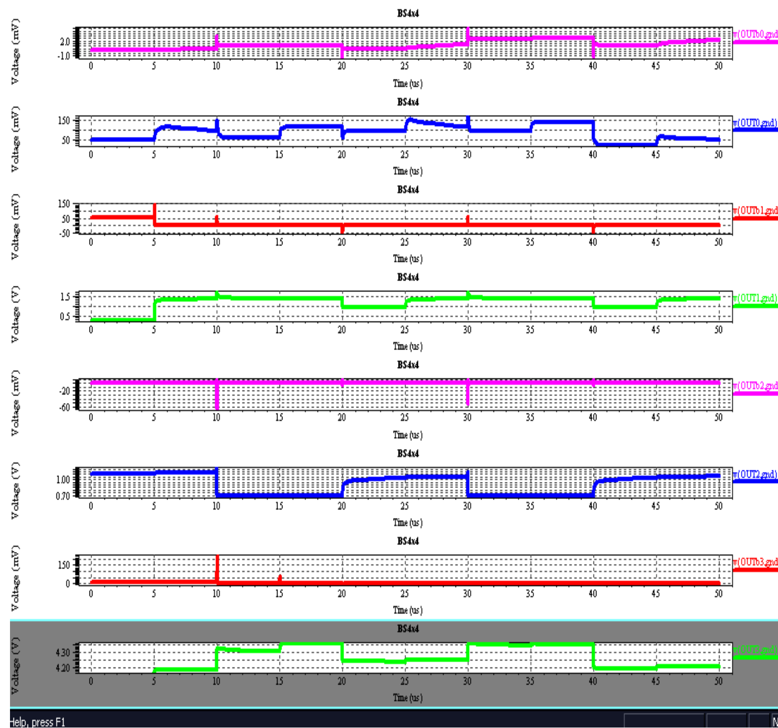

Figure 6. Simulation of 4X4 SRAM cell for 8T Memory cell

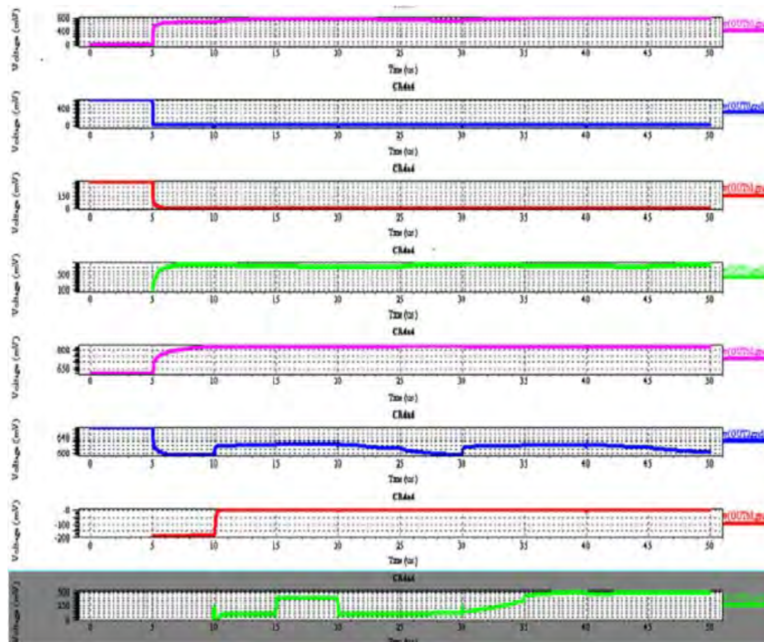

Figure 7. Simulation result of 10T SRAM memory cell

TABLE I. POWER CALCULATIONS OF 8T SRAM CELL

Temperature (°C)	Transient Analysis time (Sec)	Total time (Sec)	Static Power (Watts)	Dynamic Power (Watts)	Total Power (Watts)	Transient Delay (Sec)
25	24.71	34.27	0.090	0.109	9.867	2.2239
45	27.39	88.28	0.139	0.221	4.838	3.8072
65	28.29	54.39	0.273	0.270	12.416	7.7231
75	59.34	66.59	0.438	0.380	21.689	25.990

TABLE II. POWER CALCULATIONS OF 10T SRAM CELL

Temperature (°C)	Transient Analysis time (Sec)	Total time (Sec)	Static Power (Watts)	Dynamic Power (Watts)	Total Power (Watts)	Transient Delay (Sec)
25	3.25	4.76	0.054	0.027	3.199	0.1755
45	3.50	4.41	0.062	0.067	3.422	0.2170
65	3.51	4.51	0.208	0.217	11.431	0.7300
75	2.75	4.00	0.385	0.217	11.431	1.0588

CONCLUTION

In this chapter,the design of read circuit with charge recycling is explained. The simulation of circuit and its waveforms of 8T and 10T SRAM memory cell also prescribed.From the simulation results it has been proved that,this circuit worked for a banked organization structure gives better response in suppressing delay and minimizing the total power consumption. For 8T and 10T SRAM memory cell dynamic power , static power and total power are calculated with various temperature by giving variable supply voltage ranging from 0 V to 33mV using 180 nm CMOS technology. It is also observed that the temperature increases from 0°C to high value the total power increases with respect to time. Dynamic and static power remains constant for greater temperature range. Transient time and delay is somehow increased.But ihis concepts only applicable to increase better performance in read operation alone. This implies that power consumed due to half-access cells during the read operation is no longer a design bottleneck and circuit designers can partition the macro differently with more cells per row, hence its layout is more efficient and can be used to compensate the area overhead induced by the larger 10T cell layout.With the help of precharge scaling techniques both read and write operation to be considered that is introduced in subsequent chapters.

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