CMOS Technology Vs Carbon Nano Scale FET's

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Abstract - Moore 's law originated in around 1970 which led us to this great concept of doubling the transistors on the single chip after every two years or 18 months, but with a limitation that if the transistors size kept on diminishing and reaches the size of an atom then how the scaling is further going to be . But this law had made possible to increase the chip density and CMOS technology came into existence and became popular over simple MOSFET technology. As we move to deep sub-micron technologies the secondary effects in CMOS starts playing its part and it becomes difficult to handle these effects in a CMOS. As evolution is never stopped, to overcome such effects at sub-micron level other technology is being used now, CNTFET, which make use of CNT's, made up of graphene.

Key Words: MOSFET (Metal Oxide Semiconductor field effect transistor), CNT (Carbon Nano Tubes), CNTFET (Carbon Nano Tube Field Effect Transistor), CMOS, Nano scale.

I. INTRODUCTION

Gordon Moore, in 1970, predicted that because of the continuous miniaturization, transistor count on the same chip would double itself in every 18 months. [1, 3] And actually his prediction turned true and now it is being treated as a law. But this law also had a limitation of what if the transistors attain the size of an atom. As by reducing the size of the transistor the speed of the device gets increased and the area gets reduced.However, with the advancement in technology the device continues to scale down leading to increased in the density. and increased performance in every technology generation, followed by "Moore's Law," [1, 2] Such an advancements has let transistors to become smaller and faster, which in turns consume less power, and are cheaper to fabricate. As the size of a transistoralso has a limit it cannot be diminished than an atom, hence scaling cannot keep on going beyond this. The first integrated circuit was made-up using bipolar technology. After the fabrication with bipolar technology MOSFET came into picture after a year later. One of the reasons behind the late arrival of the MOS was its integral instability, because the dielectric of gate in a MOS consists some infinitesimal amount of alkali element which could cause the shift in the threshold voltage of the transistor during its operation. The problem with BJT's is that they consumes a lot of power even when the transistors are switched 'OFF', the quantity of the leakage current in BJT's is somewhat sizeable. The solution to this problem was MOS technology which eventually made its way [3].Scaling the dimensions of MOS devices is easier than any other transistor technology. [3, 4, 5, 6] MOS technology acquired its evolution and in late eighties, CMOS processes were widely adopted. Present day integrated circuits would nothave been survived if the CMOS technology would not have been acknowledged and implemented around the late eighties. The most significant parameters of a CMOS devices is high noise immunity and low static power. When Cmos devices are switching in on and off state only then the considerable amount of power is drawn. Resulting, CMOS devices bring forth little heat than any another technology. [3, 5] Present the progresses have gone to the researches of nanoscale devices. Nanoscale devices deals with the size of 100nm and lesser than that. phenomena such as quantum confinement and single-electron effects in electronics starts gearing up at such sizes. Along with this other effects which become dominant are near-field behavior in optics and electromagnetics, single-domain effects in magnetics etc. [3] There are a variety of devices working at nanoscale which can easily replace present CMOS circuits. These Nano electric devices include nanowire or carbon nanotube transistors, graphene FETs, single electron transistors, and spin transistors.[3,6] Out of all these nano electronic devices CNT FET's will be discussed in this paper, where carbon nano tubes are used as the bulk channel material instead of silicon which is always being used in the conventional CMOS technology. These FET's have a good control all over arrangement, it has a better threshold voltage, improved sub threshold slope , High electron mobility , High current density and High trans conductance.

II. CMOS TECHNOLOGY OVERVIEW

CMOS stands for Complementary Metal Oxide Semiconductor. A CMOS has a unique design style, some times also called as complementary symmetric, as it uses complementary and bilateral twain of p-type MOSFET and n-type MOSFET [8] The most important parameters of CMOS are high noise immunity and low static power consumption. This happens due to the series combination draws significant power only momentarily during switching between on and off states as Since one transistor of the pair is always off, in result to this, CMOS devices produce less amount of heat than any other logics. Unlike any other technology like transistor–transistor

logic (TTL) or NMOS logic, lesser amount of heat is wasted. When the state of the device is not changed, still such types of logics have some standing current. Due to CMOS technology a galactic denseness of logic can be enforced on the very chip. This has been among the utmost reasons that CMOS became the most used technology to be implemented in VLSI chips.

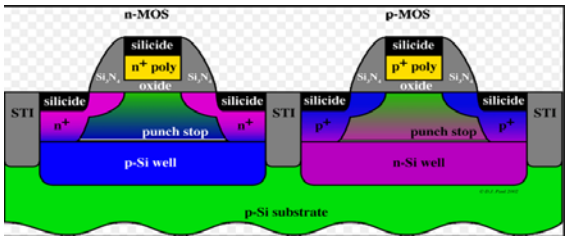

Figure 1: A Cross Sectional View of CMOS

The DC power is not consumed due to the absence of a strictly resistive path to ground. The symmetry of the device is maintained due to the pull-up and pull-down resistances of the P- and N-channel transistors which are made equal.

The fabrication of CMOS is very difficult than the fabrication of a single NMOS transistor as in CMOS there are two different types of transistors which are made on the single substrate as shown in figure 1. shows a set of transient output characteristics for a typical CMOS inverter are shown in Figure 2. In this example the NMOS pull-down transistor has the marginal channel length and width of 3µ, while the PMOS pull-up transistor has a channel width of almost double that of NMOS. The output load for the inverter is another identical inverter, and the input is a pulse with a 1 n [5, 8].

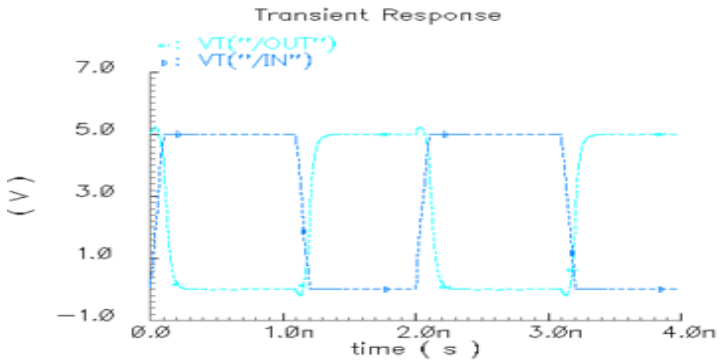

Figure 2: Transient Output for a Typical CMOS Inverter

Among the similar feature sizes the CMOS technology is said to be the cheapest. There are many resources available in the CMOS technology. CMOS technology can be further scaled down as per the technology. [3,8] It draws a very little amount of power at low frequency. CMOS technology can be used for mixed signals (digital and analog) together as well, on a single chip. CMOS technology integrates large number of transistors on the single chip. On the other hand CMOS consumes a lot of power at high frequency and the transconductance of CMOS are very low than BJT [3, 8, 9]. But on the other hand the switch of a CMOS inverter is kept on for a long time hence it can be damaged easily. There is a large propagation delay due to the lump capacitance involved with it. The noise margin in CMOS are also low. [3, 8, 10]

III. CHALLENGES WITH NANOSCALE MOSFETs

Nanoscale MOSFET's provides us with useful interpretation of the anomalies that we might encounter in their SPICE simulations, these SPICE tools also let us know the future trends and the limitations of the scaling of the device. In the next section, we are going to put emphasis on these phenomena. We will start of with the introduction to the overview of scaling trend of silicon-based planar bulk MOSFETs and spot light the challenges to be solved. On going approaches to control all thse small-geometry effects such as increased leakage currents, threshold voltage variations, weakened gate controllability over the channel, and increased in S/D resistances will be discussed.[8]

IV. CARBON NANO TUBES FET

Carbon nanotubes (CNTs) were recognized in late nineties, CNT's are allotropes of carbon having a cylinder like structure.The length-to-diameter ratio of nano tubes is up to 132,000,000:1. There are certain unique properties about these cylindrical carbon molecules [11], the thermal conductivities , mechanical and electrical properties of CNT's are quite extraordinary which make them very important for nanotechnology, Carbon Nano tubes are used in various area's like electronics, optics and in number of fields of materials science and technology. Carbon

Nano tubes uses thick sheets of carbon called graphene, CNT belong to the fullerene family and their name is inspired by their long and hollow structure .

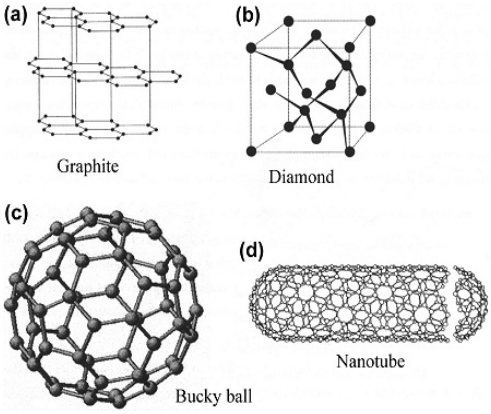

Figure 3: Allotropes of Carbon

These carbon nanotubes can be of metals or semiconductors depending upon the method on which it is rolled. These sheets are rolled at specific and discrete angles, which are called as chiral. And the combo rolling angle and radius decides the nanotube properties. The way CNT's are rolled is called its chirality. There is an advantage with the nanotubes that their threshold voltage can be easily controlled. The band gap of CNT and their diameter are inversely proportional to each other so either can be controlled by varying the other. Band gap of CNT's are inversely proportional to their diameters. [7, 10].

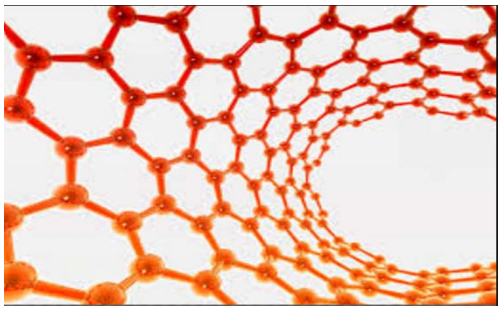

Figure 4: Carbon Nano Tube

The Carbon Nano tubes have great strength precisely due to the nature of bonds they inherit .The chemical bonding of nanotubes is composed entirely of sp^2 bonds, which is same as that found in graphite. These sp^2 bonds are stronger than the sp^3 bonds which are generally found in alkanes and diamond. Due to the qualities like have high thermal conductivity, current carrying capacity, and excellent mechanical and thermal stability nanotubes can be used as interconnects in the future .[12] now importantly these CNT's are used in CNTFET (carbon nanotube field-effect transistor), these transistors use CNT's as the channel material instead of silicon which is used in routine CMOS technology. CNTFET have a single carbon nanotube or an array of carbon nanotubes as the channel material.

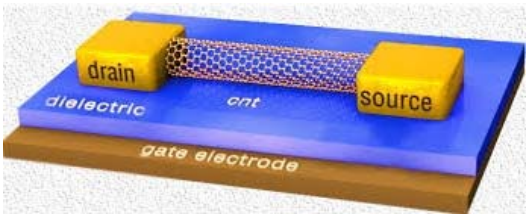

Figure4: A CNTFET, With Carbon Nanotube as Channel Material

Now the challenges come into existence when the technology goes to 22nm and so. At this very channel length fabrication and device performance issues comes into picture. [13]When we talk about CMOS technology there are a number of limitations that a device has to face as the technology shrunk, few of the, electron tunneling through short channels and thin insulator films, variations in device structure and doping, leakage currents, passive power dissipation, short channel effects etc. [14] These secondary effects can be reduced by using CNT's as channel material, where one of the ways is to use CNTFET's. one of the greatest feature in Carbon Nano tube is that there is no is no boundary scattering because of the lack of boundaries in the perfect and hollow cylinder

structure of CNTs. CNT's allow only forward and back ward scattering as the material they use is quasi-1D.These properties make CNT a reliable material to be used in future.[15]Due to the strong covalent carbon–carbon bonding, with sp2 configuration, makes carbon nanotubes chemically inert. Also carbon nanotubes are able to transport large amounts of electric current. Carbon nanotubes are also able to conduct heat nearly as well as diamond or sapphire, and due to their miniaturized dimensions, the CNTFET uses much less power than a silicon-based device and have high speeds [16].

V. CONCLUSION

CNT's are inert in nature due to the bonding arrangement and nature of bonds CNTFET's are capable of bearing various fabrications and device challenges, few of them are electron tunneling through short channels and thin insulator films, variations in the structure of device and doping, leakage currents, passive power dissipation, short channel effects etc. because of inert nature of CNT material used they have high thermal conductivity, current carrying capacity, and excellent mechanical and thermal stability .

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